IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Frederick S. DUNLAP, et al.

For: SYSTEM AND METHOD FOR FORCING AN SRAM INTO A KNOWN STATE DURING POWER-UP

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The Board of Patent Appeal and Interferences
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

BRIEF IN SUPPORT OF APPEAL

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This brief contains these items under the following headings, and in the order set forth below (37 C.F.R. § 41.37(c)(1)):

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The final page of this brief before the beginning of the Appendix of Claims bears the attorney's signature.

I. REAL PARTY IN INTEREST (37 C.F.R. § 41.37(c)(1)(i))

The real party in interest in this appeal is Advanced Micro Devices, Inc., the assignee, as evidenced by the assignment recorded at Reel 015217, Frame 0200.

II. RELATED APPEALS AND INTERFERENCES (37 C.F.R. § 41.37(c)(1)(ii))

There are no interferences or other appeals that will directly affect, or be directly affected by, or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS (37 C.F.R. § 41.37(c)(1)(iii))

A. TOTAL NUMBER OF CLAIMS IN APPLICATION

There are twenty (20) claims pending in the application (claims 1-20).

B. STATUS OF ALL THE CLAIMS

1. Claims pending:

   Claims 1-20.

2. Claims withdrawn from consideration but not canceled:

   NONE.

3. Claims allowed:

   NONE.

4. Claims objected to:

   NONE.

5. Claims rejected:

   Claims 1-9 and 11-19 are rejected under 35 U.S.C. § 102(b).

Claims 10 and 20 are rejected under 35 U.S.C. § 103(a).

6. Claims canceled:

Claims 21 and 22.

C. CLAIMS ON APPEAL

There are two (2) claims on appeal, claims 10 and 20.

IV. STATUS OF AMENDMENTS (37 C.F.R. § 41.37(c)(1)(iv))

Amendments to claims 1 and 11 to incorporate the additional features of dependent claims 10 and 20, respectively, were submitted subsequent to the final office action dated December 13, 2004 (hereinafter, "the Final Rejection"). The cancellation of claims 10 and 20 and the addition of new claims 23-26 were submitted in the same amendment subsequent to the Final Rejection. The advisory action dated March 7, 2005 (hereinafter, "the Advisory Action") indicated that the amendments would not be entered as they allegedly raise new issues that would require further consideration and/or search and were deemed by the Examiner as not placing the application in better form for appeal by materially reducing or simplifying the issues for appeal. The Applicants traversed the refusal to enter the amendments on the grounds that the amendments do in fact place the application in better form for appeal by reducing and simplifying the issues for appeal. A Petition under 37 C.F.R. Section 1.181 (hereinafter, "the Petition") was submitted with the Notice of Appeal on May 12, 2005 to invoke the supervisory authority of the Director to direct entry of the claim amendments submitted after the Final Rejection. At the time of the submission of this Brief, the status of the Petition is unknown. The remarks herein therefore are provided based on an assumption that the amendments were not entered pursuant to the Petition. However, in the event that the amendments are entered, the

merits of the statements made herein are applicable to claims 1 and 11 amended to recite the additional features of appealed dependent claims 10 and 20, respectively.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER (37 C.F.R. § 41.37(c)(1)(v))

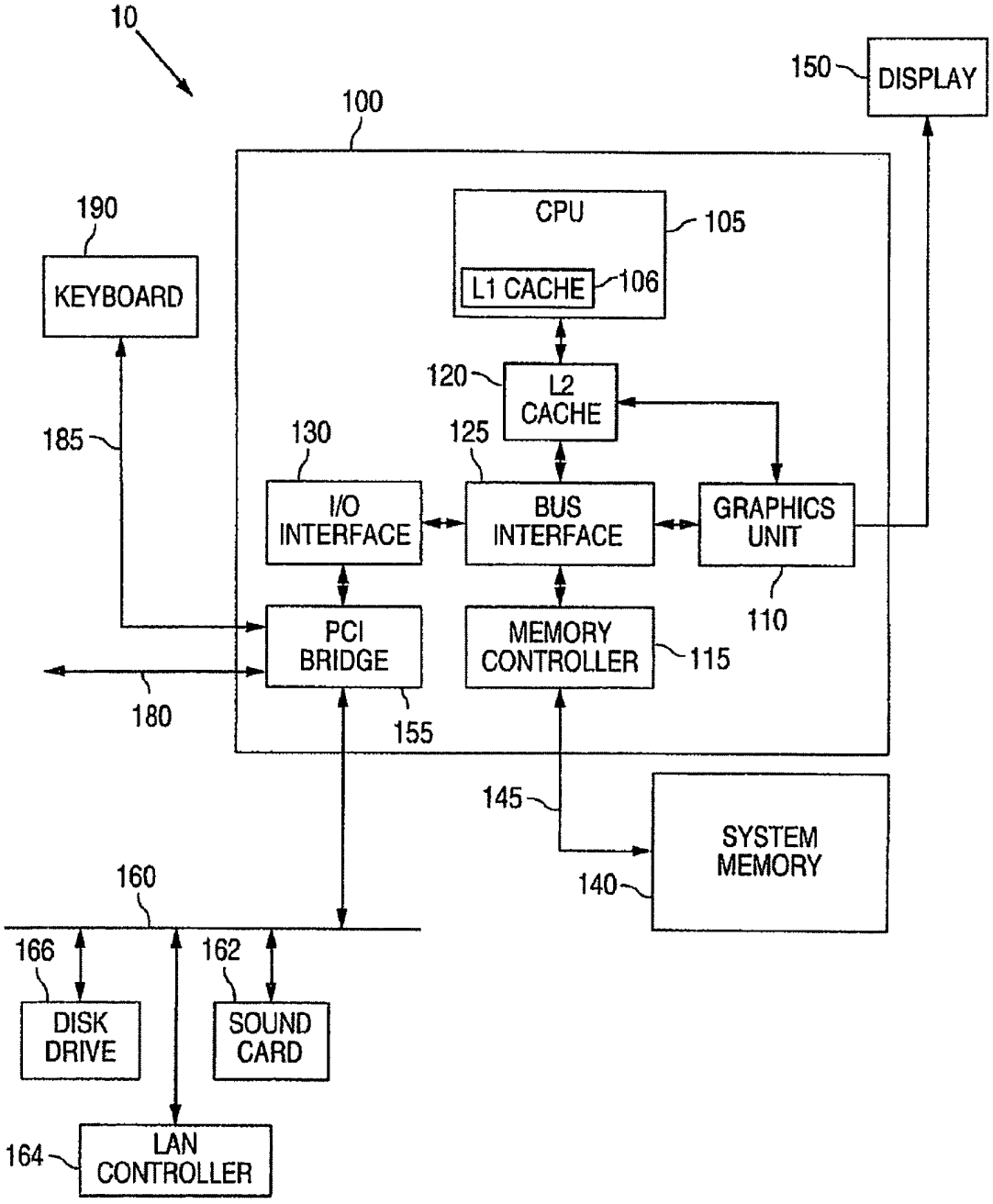
The following summary is provided to give the Board the ability to quickly determine where the claimed subject matter appealed herein is described in the present application and is not to limit the scope of the claimed invention.

Claim 1 recites the features of a static random access memory (SRAM) device capable of storing a program that is accessible when said SRAM device is powered up. Claim 1 provides that the SRAM device comprises a plurality of storage cells, each of said storage cells comprising a data latch having a first input/output (I/O) line and a second I/O line. Claim 1 further provides that the data latch comprises a first inverter having an input coupled to said first I/O line and an output coupled to said second I/O line, a second inverter having an input coupled to said second I/O line and an output coupled to said first I/O line, and a biasing circuit capable of forcing at least one of said first and second I/O lines to a known logic state when power is applied to said SRAM device, wherein said known logic state comprises a portion of said program. Claim 10, which depends from claim 1, recites the additional features of wherein said biasing circuit comprises a grounding circuit selectively connected by a programmable connect to one of said first inverter output and said second inverter output, wherein said grounding circuit is temporarily enabled after power is applied to said SRAM device, thereby grounding one of said first inverter output and said second inverter output and forcing said second I/O line to said known logic state.

Claim 11 recites the features of a data processor comprising a central processing unit (CPU) capable of executing a boot-up program when power is applied to said CPU. Claim 11 provides that the CPU comprises a static random access memory (SRAM) device capable of storing said boot-up program, said SRAM device comprising a plurality of storage cells capable of storing said boot-up program. Claim 11 further provides that each of the storage cells comprises a data latch having an input and an output, said data latch comprising a first inverter having an input coupled to said first I/O line and an output coupled to said second I/O line and a second inverter having an input coupled to said second I/O line and an output coupled to said first I/O line. Claim 11 further provides that the data latch comprises a biasing circuit capable of forcing at least one of said first and second I/O lines to a known logic state when power is applied to said SRAM device, wherein said known logic state comprises a portion of said boot-up program. Claim 20, which depends from claim 11, recites the additional features of wherein said biasing circuit comprises a grounding circuit selectively connected by a programmable connect to one of said first inverter output and said second inverter output, wherein said grounding circuit is temporarily enabled after power is applied to said SRAM device, thereby grounding one of said first inverter output and said second inverter output and forcing said second I/O line to said known logic state.

Figures 1-3 of the present application and their corresponding disclosure are illustrative of an exemplary embodiment of the subject matter of claims 1, 10, 11 and 20. Figure 1 (reproduced below) illustrates an exemplary microprocessor 100 including a CPU 105. The CPU 105 includes an L1 cache 106 that "may comprise a plurality of SRAM cells that may be biased (or initialized) to a particular logic state (Logic 1 or Logic 0) during a power reset." The Present

Application, p. 12, lines 3-6. The L2 cache 120 also may comprise a plurality of SRAM cells that can be similarly biased or initialized. See Id., p. 12, lines 17-19.

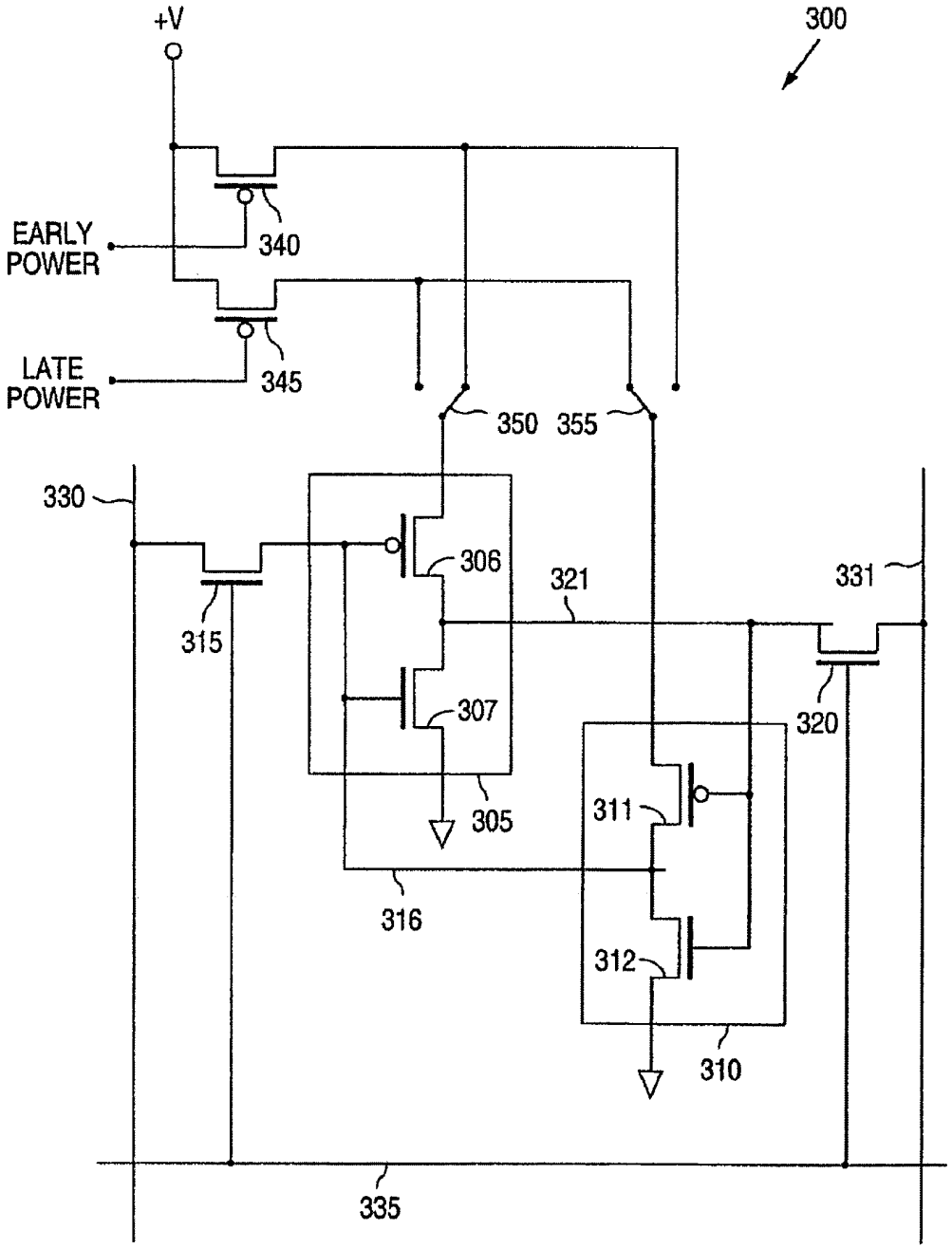


The Present Application, Figure 1

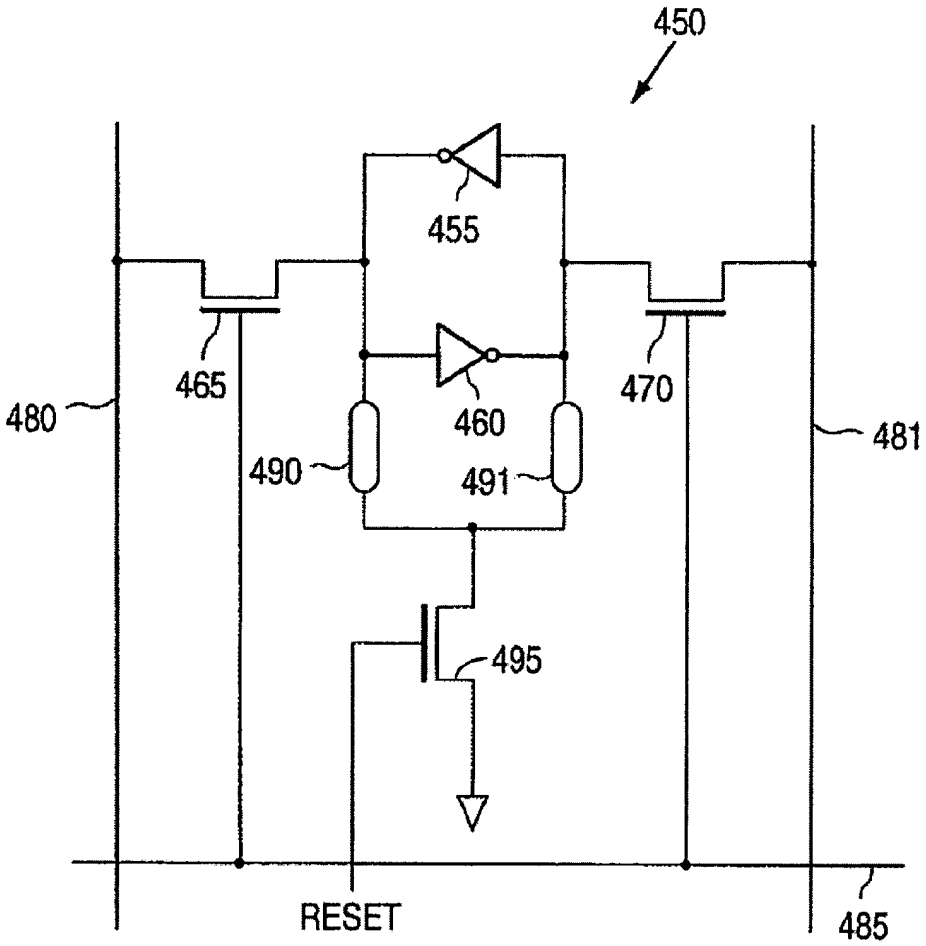
Figure 2 (reproduced below) illustrates an exemplary SRAM cell 300 that may be used in the L1 cache 106 or the L2 cache 120 of Figure 1. As shown by Figure 2, the SRAM cell 300 includes CMOS inverters 305 and 310, column line 331, row line 335 and p-type MOS transistors 340 and 345. The SRAM cell 300 also includes programmable contacts 350 and 355, either of which can be connected during fabrication or manufacture to transistor 340 or transistor 345. See Id., p. 13, lines 8-10. The output line 321 of the inverter 305 is connected to the input of the inverter 310 and the output line of the inverter 310 is connected to the input of the inverter 305 so as to form a latch for data storage. See Id., p. 13, lines 19-22. The inverters 305 and 310 are connected to a power supply rail via power transistors 340 and 345 via programmable contacts 350 and 355. See Id., p. 14, lines 1-8. The passage at p. 14, line 8 to p. 17, line 10 describes an exemplary sequence for the application of power at startup and the use of the column line 331, the row line 335 and the programmable contacts 350 and 355 so as to allow the SRAM cell 300 store, for example, a bit value of a boot-up program while also permitting the SRAM cell 300 to act as a conventional SRAM cell after power-up/boot-up.

Figure 3 (reproduced below) illustrates another exemplary SRAM cell 450 that may be implemented as part of the L1 cache 106 or the L2 cache 120 of Figure 1. The SRAM cell 450 comprises inverters 455 and 460, n-type MOS transistors 465, 470 and 495, column line 480, column line 481, row line 485 and programmable connects 490 and 491. See Id., p. 17, lines 10-23. One of the programmable connect 490 or the programmable connect 491 may be removed (or not installed) during fabrication to cause the SRAM cell 450 to have a particular logic value (Logic 1 or Logic 0) as the initial power-up state. See Id., p. 18, lines 1-7. The passage at p. 18, line 8 to p. 19, line 10 describes an exemplary sequence for the application of power at startup and the use of the RESET line, the column lines 480 and 481, the row line 485 and the

programmable connects 490 and 491 so as to allow the SRAM cell 450 store, for example, a bit value of a boot-up program while also permitting the SRAM cell 450 to act as a conventional SRAM cell after power-up/boot-up.



The Present Application, Figure 2



The Present Application, Figure 3

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL (37 C.F.R. § 41.37(c)(1)(vi))

Claims 10 and 20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over the U.S. Patent No. 5,365,475 to Matsumura *et al.* (hereinafter "the Matsumura reference") in view of U.S. Patent No. 6,208, 350 to Shimazu *et al.* (hereinafter, "the Shimazu reference") as set forth in the Final Rejection.

VII. ARGUMENTS (37 C.F.R. § 41.37(c)(1)(vii))

Based on the arguments and issues below, claims 10 and 20 do no stand and fall together. In addition to having different scopes, each of claims 10 and 20 has a unique set of issues relating to its rejection and appeal as indicated in the arguments below:

Rejection of Claims 10 and 20 under 35 U.S.C. § 103(a)

In Section 5 of the Final Rejection, claims 10 and 20 (which depend from claims 1 and 11, respectively) were rejected under 35 U.S.C. § 103(a) as unpatentable over the Matsumura reference in view of the Shimazu reference. For ease of reference, claims 1, 10, 11 and 20 are reproduced below:

> 1. (Original) A static random access memory (SRAM) device capable of storing a program that is accessible when said SRAM device is powered up, said SRAM device comprising a plurality of storage cells, each of said storage cells comprising:
> a data latch having a first input/output (I/O) line and a second I/O line, said data latch comprising:
> a first inverter having an input coupled to said first I/O line and an output coupled to said second I/O line; and
> a second inverter having an input coupled to said second I/O line and an output coupled to said first I/O line; and
> a biasing circuit capable of forcing at least one of said first and second I/O lines to a known logic state when power is applied to said SRAM device, wherein said known logic state comprises a portion of said program.
>
> 10. (Original) The SRAM device as set forth in Claim 1 wherein said biasing circuit comprises a grounding circuit selectively connected by a programmable connect to one of said first inverter output and said second inverter output, wherein said grounding circuit is temporarily enabled after power is applied to said SRAM device, thereby grounding one of said first inverter output and said second inverter output and forcing said second I/O line to said known logic state.

11. (Previously Presented) A data processor comprising a central processing unit (CPU) capable of executing a boot-up program when power is applied to said CPU, said CPU comprising:
a static random access memory (SRAM) device capable of storing said boot-up program, said SRAM device comprising a plurality of storage cells capable of storing said boot-up program, each of said storage cells comprising:
a data latch having an input and an output, said data latch comprising:
a first inverter having an input coupled to said first I/O line and an output coupled to said second I/O line; and
a second inverter having an input coupled to said second I/O line and an output coupled to said first I/O line; and
a biasing circuit capable of forcing at least one of said first and second I/O lines to a known logic state when power is applied to said SRAM device, wherein said known logic state comprises a portion of said boot-up program.

20. (Original) The data processor as set forth in Claim 11 wherein said biasing circuit comprises a grounding circuit selectively connected by a programmable connect to one of said first inverter output and said second inverter output, wherein said grounding circuit is temporarily enabled after power is applied to said SRAM device, thereby grounding one of said first inverter output and said second inverter output and forcing said second I/O line to said known logic state.

According to 35 U.S.C. § 103(a), "[a] patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains."

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing *a prima facie* case of obviousness. In re Fritch, 972 F.2d 1260,1262,23 U.S.P.Q. 2d 1780, 1783 (Fed. Cir. 1992). The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention is always upon the Patent Office. In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Piasecki, 745 F.2d 1468, 1472,

223 U.S.P.Q. 785, 788 (Fed. Cir. 1984). Only when a *prima facie* case of obviousness is established does the burden shift to the applicant to produce evidence of nonobviousness. In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Rijckaert, *9* F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of a patent. In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Grabiak, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. In re Bell, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim features. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. Id.

The Final Rejection asserts that the proposed combination of the Matsumura reference and the Shimazu reference discloses or suggests the features of claims 10 and 20. In contrast with the assertions of the Final Rejection, the proposed combination of the Matsumura and Shimazu references fails to disclose or suggest at least one feature of each of claims 10 and 20 and therefore fails to disclose or suggest each and every feature of claims 10 and 20.

A. Rejection of Claim 10

Claim 1, from which claim 10 depends, recites the features of a static random access memory (SRAM) device comprising a plurality of storage cells, each of said storage cells comprising a data latch having a first input/output (I/O) line and a second I/O line. Claim 1 further provides that said data latch comprises a first inverter having an input coupled to said first I/O line and an output coupled to said second I/O line and a second inverter having an input coupled to said second I/O line and an output coupled to said first I/O line. Claim 1 further recites the features of a biasing circuit capable of forcing at least one of said first and second I/O lines to a known logic state when power is applied to said SRAM device, wherein said known logic state comprises a portion of said program. Claim 10 recites the additional features of wherein said biasing circuit comprises a grounding circuit selectively connected by a programmable connect to one of said first inverter output and said second inverter output, wherein said grounding circuit is temporarily enabled after power is applied to said SRAM device, thereby grounding one of said first inverter output and said second inverter output and forcing said second I/O line to said known logic state.

1) The Proposed Combination of the Matsumura and Shimazu References Fails to Disclose or Suggest the Grounding Circuit Feature as Recited by Claim 10

The Final Rejection asserts that the Matsumura and Shimazu references, if combined as proposed, disclose the features of claim 10. Specifically, the Final Rejection asserts that the Matsumura reference discloses each and every feature of claim 1, but the Final Rejection acknowledges that the Matsumura reference fails to disclose or suggest the additional features of claim 10. The Final Rejection, pp. 5-6. The Final Rejection therefore turns to the Shimazu reference and asserts that the passage of the Shimazu reference at col. 3, line 65 to col. 4, line 14

discloses these features. Id., p. 6. For ease of reference, this relied-upon passage of the Shimazu reference is provided below:

> As described above, in the embodiment of FIG. 3, the ratio latch 4 can be set by merely raising the output voltage of the power source 12 which is driving the memory circuit 14 higher than the output voltage at the ordinary operation. Accordingly, there is neither the necessity of wiring the set signal input line for transmitting a set initialization signal, nor the necessity of the set initialization signal input terminal, thereby enabling the implementation of a larger scale integration.
>
> Meanwhile, the switching of the output voltage of the power source 12 is readily performed by forming a power supply circuit (not shown) provided in the outside of the memory circuit 14 in such a way that it could output two different voltages.
>
> As for the MOS transistor 15, such a device as having sufficient driving capability to pull down the level of the input data line to "0" even when the input data is "1" may be used.

The Shimazu Reference, col. 3, line 65-col. 4, line 14.

Neither the relied-upon passage of the Shimazu reference nor any other passage of the Shimazu reference discloses or suggests a grounding circuit *selectively* connected *by a programmable select* to one of a first inverter output or a second inverter output as recited by claim 10. Instead, Figure 3 of the Shimazu reference and the above relied-upon passage of the Shimazu reference merely disclose a transistor 15 *fixedly* coupled to the output of the inverter 3 at one node and to ground at another. The Shimazu reference fails to disclose or suggest that the transistor 15 (which the Final Rejection appears to consider equivalent to the grounding circuit limitation of claim 10) is *selectively* connected to one of the outputs of the inverters 2 and 3 as recited by claim 10. Moreover, the Shimazu reference provides no disclosure or suggestion that the transistor 15 is connected to the output of the inverter 3 by a *programmable connect*, so the Shimazu reference necessarily fails to disclose or suggest a grounding circuit *selectively* connected by a *programmable connect* as recited by claim 10.

2) The Proposed Combination of the Matsumura and Shimazu References Fails to Disclose or Suggest Temporarily Enabling the Grounding Circuit as Recited by Claim 10

Claim 10 recites the features of wherein said grounding circuit is temporarily enabled after power is applied to said SRAM device, thereby grounding one of said first inverter and said second inverter output and forcing said second I/O line to said known logic state. As described above, the Final Rejection asserts that the transistor 15 of the Shimazu reference is equivalent to the grounding circuit feature of claim 10 and that the relied-upon passage of the Shimazu reference (reproduced above) discloses the temporary enabling feature of claim 10. Even if it is assumed, *arguendo*, that the transistor 15 of the Shimazu reference actually is equivalent to the grounding circuit feature of claim 10 (which it is not), neither the relied-upon passage of the Shimazu reference nor any other passage of the Shimazu reference provides any disclosure or suggestion related to temporarily enabling the transistor 15 after power is applied to the memory cell. Accordingly, the Shimazu reference, alone or in combination with the Matsumura reference, fails to disclose or suggest the features of wherein said grounding circuit is temporarily enabled after power is applied to said SRAM device as recited by claim 10.

3) The Combination of the Matsumura and Shimazu References is Improper

Not only does the proposed combination of the Matsumura reference and the Shimazu reference fail to disclose or suggest numerous features of claim 10, there is no motivation to combine the teachings of the Matsumura reference and the Shimazu reference as proposed by the Final Rejection. The Matsumura reference teaches a technique whereby the inputs and outputs of two inverters of a memory cell are connected in various ways to two ground lines (G1, G2) and two supply lines (V1, V2) so as to configure the memory cell to be a ROM cell storing a value of 1, a ROM cell storing a value of 0 or a RAM cell depending on the particular connection

to the lines and the voltages applied to the lines. See, e.g., The Matsumura Reference, Figures 3-8A. In contrast, the Shimazu reference teaches a technique whereby signal lines (e.g., set signal 7a of "prior-art" Figure 1 or reset signal 13a of "prior-art" Figure 2) may be omitted by varying the voltage of a power supply that powers the entire memory cell so as to cause a transistor to source the input of an inverter to logic high or low depending on the particular configuration. Thus, while the Matsumura reference teaches using supply lines so as to configure a memory cell to function in a certain manner, the Shimazu reference teaches the avoidance of such supply lines. Accordingly, the combination of the Matsumura and Shimazu references as proposed by the Final Rejection relies on the irreconcilable teachings of the use of such supply lines as taught by the Matsumura reference and the elimination of such lines as taught by the Shimazu reference.

4) Claim 10 is Allowable under 35 U.S.C. § 103(a)

As described in sections 1-3 above, there is no motivation to combine the Matsumura and Shimazu references, and even if so combined, the combination of the Matsumura and Shimazu references fails to disclose or suggest each and every feature of claim 10. Accordingly, the Final Rejection fails to establish a *prima facie* case of obviousness in support of its rejection of claim 10 under 35 U.S.C. § 103(a). Claim 10 therefore is allowable under 35 U.S.C § 103(a).

B. Rejection of Claim 20

Claim 11, from which claim 20 depends, recites the features of a data processor comprising a central processing unit (CPU) capable of executing a boot-up program when power is applied to said CPU. Claim 11 further recites the features of the CPU comprising a static random access memory (SRAM) device capable of storing said boot-up program, said SRAM

device comprising a plurality of storage cells capable of storing said boot-up program. In addition, claim 11 provides that each of the storage cells comprise a data latch having an input and an output, said data latch comprising a first inverter having an input coupled to said first I/O line and an output coupled to said second I/O line and a second inverter having an input coupled to said second I/O line and an output coupled to said first I/O line. Claim 11 also provides that each storage cell further comprises a biasing circuit capable of forcing at least one of said first and second I/O lines to a known logic state when power is applied to said SRAM device, wherein said known logic state comprises a portion of said boot-up program. Claim 20 recites the additional features of wherein said biasing circuit comprises a grounding circuit selectively connected by a programmable connect to one of said first inverter output and said second inverter output, wherein said grounding circuit is temporarily enabled after power is applied to said SRAM device, thereby grounding one of said first inverter output and said second inverter output and forcing said second I/O line to said known logic state.

1) The Proposed Combination of the Matsumura and Shimazu References Fails to Disclose or Suggest the Grounding Circuit Feature as Recited by Claim 20

The Final Rejection asserts that the Matsumura and Shimazu references, if combined as proposed, disclose the features of claim 20 under the same rationale as the rejection of claim 10. As described above, the Final Rejection acknowledges that the Matsumura reference fails to disclose or suggest the additional features of claim 20 and therefore turns to the Shimazu reference and asserts that the passage of the Shimazu reference at col. 3, line 65 to col. 4, line 14 (reproduced above) discloses these features. The Final Rejection, pp. 5-6.

Neither the relied-upon passage of the Shimazu reference nor any other passage of the Shimazu reference discloses or suggests a grounding circuit *selectively* connected *by a*

programmable select to one of a first inverter output or a second inverter output as recited by claim 20. Instead, Figure 3 of the Shimazu reference and the above relied-upon passage of the Shimazu reference merely disclose a transistor 15 *fixedly* coupled to the output of the inverter 3 at one node and to ground at another. The Shimazu reference fails to disclose or suggest that the transistor 15 (which the Final Rejection appears to consider equivalent to the grounding circuit limitation of claim 20) is *selectively* connected to one of the outputs of the inverters 2 and 3 as recited by claim 20. Moreover, the Shimazu reference provides no disclosure or suggestion that the transistor 15 is connected to the output of the inverter 3 by a *programmable connect*, so the Shimazu reference necessarily fails to disclose or suggest a grounding circuit *selectively* connected by a *programmable connec*t as recited by claim 20.

2) The Proposed Combination of the Matsumura and Shimazu References Fails to Disclose or Suggest Temporarily Enabling the Grounding Circuit as Recited by Claim 20

Claim 20 recites the features of wherein said grounding circuit is temporarily enabled after power is applied to said SRAM device, thereby grounding one of said first inverter and said second inverter output and forcing said second I/O line to said known logic state. As similarly described above, the Final Rejection asserts that the transistor 15 of the Shimazu reference is equivalent to the grounding circuit feature of claim 20 and that the relied-upon passage of the Shimazu reference (reproduced above) discloses the temporary enabling feature of claim 20. Even if it is assumed, *arguendo*, that the transistor 15 of the Shimazu reference actually is equivalent to the grounding circuit feature of claim 20 (which it is not), neither the relied-upon passage of the Shimazu reference nor any other passage of the Shimazu reference provides any disclosure or suggestion related to temporarily enabling the transistor 15 after power is applied to the memory cell. Accordingly, the Shimazu reference, alone or in combination with the

Matsumura reference, fails to disclose or suggest the features of wherein said grounding circuit is temporarily enabled after power is applied to said SRAM device as recited by claim 20.

3) The Proposed Combination of the Matsumura and Shimazu References Fails to Disclose or Suggest a CPU Comprising a SRAM Device

Claim 20 recites the feature of a CPU comprising an SRAM device. The Final Rejection does not address this feature of claim 20. The Shimazu reference makes no mention of a CPU in any manner. Figure 15 of the Matsumura reference discloses a microprocessor 104 having a CPU 105 and a program memory 106. However, as illustrated by Figure 15, the program memory 106 is separate from the CPU 105 and the related disclosure of the Matsumura reference provides no disclosure or suggestion that the program memory 106 can be implemented as part of the CPU 105. Accordingly, the Matsumura reference and the Shimazu reference, alone or in combination, fail to disclose or suggest a CPU comprising an SRAM device.

4) The Combination of the Matsumura and Shimazu References is Improper

Not only does the proposed combination of the Matsumura reference and the Shimazu reference fail to disclose or suggest numerous features of claim 20, for the reasons described above in section (A)(3), there is no motivation to combine the teachings of the Matsumura reference and the Shimazu reference as proposed by the Final Rejection.

5) Claim 20 is Allowable under 35 U.S.C. § 103(a)

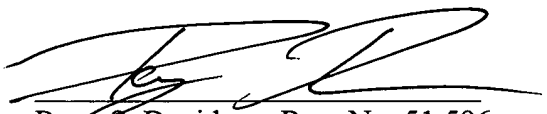
As described in sections 1-4 above, there is no motivation to combine the Matsumura and Shimazu references, and even if so combined, the combination of the Matsumura and Shimazu references fails to disclose or suggest each and every feature of claim 20. Accordingly, the Final Rejection fails to establish a *prima facie* case of obviousness in support of its rejection of claim 20 under 35 U.S.C. § 103(a). Claim 20 therefore is allowable under 35 U.S.C § 103(a).

VIII. CONCLUSION

For at least the reasons given above, at least claims 10 and 20 are allowable and the Appellants therefore respectfully request reconsideration and allowance of claims 10 and 20 and entry of the amendments submitted after the Final Rejection.

Respectfully submitted,

8 July 2005
Date



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IX. APPENDIX OF CLAIMS INVOLVED IN THE APPEAL (37 C.F.R. § 41.37(c)(1)(viii))

The text of each claim involved in the appeal is as follows:

1. (Original) A static random access memory (SRAM) device capable of storing a program that is accessible when said SRAM device is powered up, said SRAM device comprising a plurality of storage cells, each of said storage cells comprising:

a data latch having a first input/output (I/O) line and a second I/O line, said data latch comprising:

a first inverter having an input coupled to said first I/O line and an output coupled to said second I/O line; and

a second inverter having an input coupled to said second I/O line and an output coupled to said first I/O line; and

a biasing circuit capable of forcing at least one of said first and second I/O lines to a known logic state when power is applied to said SRAM device, wherein said known logic state comprises a portion of said program.

2. (Original) The SRAM device as set forth in Claim 1 wherein said biasing circuit initially applies power only to said first inverter.

3. (Original) The SRAM device as set forth in Claim 2 wherein said initial application of power only to said first inverter forces said first inverter output to a Logic 1 state.

4. (Original) The SRAM device as set forth in Claim 3 wherein said biasing circuit subsequently applies power to said second inverter.

5. (Original) The SRAM device as set forth in Claim 4 wherein said subsequent application of power to said second inverter forces said second inverter output to a Logic 0 state.

6. (Original) The SRAM device as set forth in Claim 1 wherein said biasing circuit initially applies power only to said second inverter.

7. (Original) The SRAM device as set forth in Claim 6 wherein said initial application of power only to said second inverter forces said second inverter output to a Logic 1 state.

8. (Original) The SRAM device as set forth in Claim 7 wherein said biasing circuit subsequently applies power to said first inverter.

9. (Original) The SRAM device as set forth in Claim 8 wherein said subsequent application of power to said first inverter forces said first inverter output to a Logic 1 state.

10. (Original) The SRAM device as set forth in Claim 1 wherein said biasing circuit comprises a grounding circuit selectively connected by a programmable connect to one of said first inverter output and said second inverter output, wherein said grounding circuit is temporarily enabled after power is applied to said SRAM device, thereby grounding one of said first inverter output and said second inverter output and forcing said second I/O line to said known logic state.

11. (Previously Presented) A data processor comprising a central processing unit (CPU) capable of executing a boot-up program when power is applied to said CPU, said CPU comprising:

a static random access memory (SRAM) device capable of storing said boot-up program, said SRAM device comprising a plurality of storage cells capable of storing said boot-up program, each of said storage cells comprising:

a data latch having an input and an output, said data latch comprising:

a first inverter having an input coupled to said first I/O line and an output coupled to said second I/O line; and

a second inverter having an input coupled to said second I/O line and an output coupled to said first I/O line; and

a biasing circuit capable of forcing at least one of said first and second I/O lines to a known logic state when power is applied to said SRAM device, wherein said known logic state comprises a portion of said boot-up program.

12. (Original) The data processor as set forth in Claim 11 wherein said biasing circuit initially applies power only to said first inverter.

13. (Original) The data processor as set forth in Claim 12 wherein said initial application of power only to said first inverter forces said first inverter output to a Logic 1 state.

14. (Original) The data processor as set forth in Claim 13 wherein said biasing circuit subsequently applies power to said second inverter.

15. (Original) The data processor as set forth in Claim 14 wherein said subsequent application of power to said second inverter forces said second inverter output to a Logic 0 state.

16. (Original) The data processor as set forth in Claim 11 wherein said biasing circuit initially applies power only to said second inverter.

17. (Original) The data processor as set forth in Claim 16 wherein said initial application of power only to said second inverter forces said second inverter output to a Logic 1 state.

18. (Original) The data processor as set forth in Claim 17 wherein said biasing circuit subsequently applies power to said first inverter.

19. (Original) The data processor as set forth in Claim 18 wherein said subsequent application of power to said first inverter forces said first inverter output to a Logic 1 state.

20. (Original) The data processor as set forth in Claim 11 wherein said biasing circuit comprises a grounding circuit selectively connected by a programmable connect to one of said first inverter output and said second inverter output, wherein said grounding circuit is temporarily enabled after power is applied to said SRAM device, thereby grounding one of said first inverter output and said second inverter output and forcing said second I/O line to said known logic state.

21. (Canceled)

22. (Canceled)

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JFW

PTO/SB/17 (12-04)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2005

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 500.00

Complete if Known	
Application Number	09/477,099
Filing Date	01/04/2000
First Named Inventor	Frederick S. DUNLAP et al.
Examiner Name	BETIT, Jacob F.
Art Unit	2164
Attorney Docket No.	1458- P04056

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 01-0365 Deposit Account Name: Advanced Micro Devices, Inc.

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☒ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

☒ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 ☒ Credit any overpayments

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

Application Type	FILING FEES Fee ($)	FILING FEES Small Entity Fee ($)	SEARCH FEES Fee ($)	SEARCH FEES Small Entity Fee ($)	EXAMINATION FEES Fee ($)	EXAMINATION FEES Small Entity Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 or, for Reissues, each claim over 20 and more than in the original patent	50	25
Each independent claim over 3 or, for Reissues, each independent claim more than in the original patent	200	100
Multiple dependent claims	360	180

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 20 or HP =	_____	x _____	= _____

HP = highest number of total claims paid for, if greater than 20

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 3 or HP =	_____	x _____	= _____

HP = highest number of independent claims paid for, if greater than 3

Multiple Dependent Claims Fee ($)	Fee Paid ($)
_____	_____

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee ($)	Fee Paid ($)
_____ - 100 =	_____	/ 50 = _____ (round up to a whole number)	x _____	= _____

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other: Filing a Brief in Support of an Appeal	500.00

SUBMITTED BY

Signature		Registration No. (Attorney/Agent) 51,596	Telephone 512-327-5515
Name (Print/Type)	Ryan S. Davidson		Date 8 July 2005

PTO/SB/21 (09-04)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission: 26

Application Number	09/477,099
Filing Date	01/04/2000
First Named Inventor	Frederick S. DUNLAP et al.
Art Unit	2164
Examiner Name	BETIT, Jacob F.
Attorney Docket Number	1458-P04056

ENCLOSURES *(Check all that apply)*

- [x] Fee Transmittal Form
  - [ ] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Reply to Missing Parts/ Incomplete Application
  - [ ] Reply to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
  - [ ] Landscape Table on CD
- [ ] After Allowance Communication to TC
- [ ] Appeal Communication to Board of Appeals and Interferences
- [x] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [x] Other Enclosure(s) (please Identify below):

Return Receipt Postcard

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	TOLER, LARSON & ABEL, LLP		
Signature			
Printed name	Ryan S. Davidson		
Date	8 July 2005	Reg. No.	51,596

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

Signature			
Typed or printed name	Judy Carey	Date	7/8/05